AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 14 line *5* and ending on page 16, line 24, with the following amended paragraph:

Fig. 1 is a circuit block diagram which illustrates one example of an optical semiconductor device according to the first embodiment; Fig. ~~2(a)~~ 2A is an explanatory view which typically ~~illustrate~~ illustrates rise characteristics and fall characteristics of a pair of differential transistors in an LD driving circuit; Fig. ~~2(b)~~ 2B is an explanatory view which illustrates a principle that the rise characteristics and the fall characteristics of the pair of differential transistors are averaged; Fig. 3 illustrates that optical signal waveforms in various patterns are photoelectrically converted to electric signals, the electric signals are passed through a band filter, and that the electric signals are overlaid; Fig. ~~4(a)~~ 4A is a graph which illustrates frequency response characteristics when the LD module shown in Fig. 1 is viewed from a distributed constant circuit; Fig. ~~4(b)~~ 4B is a graph which illustrates frequency response characteristics when respective bias circuits are set to have different impedances; Fig. 5 is a circuit block diagram which illustrates one example of the optical semiconductor device according to the second embodiment; Fig. ~~6(a)~~ 6A is a top view of a filter; Fig. ~~6(b)~~ 6B is an illustration of this filter viewed from an arrow P direction; Fig. 7 is a graph which compares frequency characteristics before and after the filter is inserted; Fig. 8 is an equivalent circuit diagram which simulates a high frequency operation of the optical semiconductor device shown in Fig. 5; Fig. ~~9(a)~~ 9A is a simplified equivalent circuit diagram which simulates a high frequency operation of a conventional semiconductor device shown in Fig. 18; Fig. ~~9(b)~~ 9B is a graph which illustrates a simulation result of the frequency response characteristics of this

equivalent circuit; Fig. 10~~(a)~~ 10A is a simplified equivalent circuit diagram which simulates the high frequency operation of the optical semiconductor device (differential lines) according to the present invention shown in Fig. 1; Fig. ~~10(b)~~ 10B is a graph which illustrates a simulation result of the frequency response characteristics of this equivalent circuit; Fig. ~~11(a)~~ 11A is a circuit block diagram which illustrates the configuration of a bias circuit in the equivalent circuit shown in Fig. ~~10(a)~~ 10A in detail; Fig. ~~11(b)~~ 11B is a graph which illustrates the simulation result of the frequency response characteristics based on circuit conditions shown in Fig. ~~11(a)~~ 11A; Fig. ~~11(c)~~ 11C is a circuit block diagram which illustrates the configuration of the bias circuit in the equivalent circuit shown in Fig. ~~9(a)~~ 9A in detail; Fig. ~~11(d)~~ 11D is a graph which illustrates the simulation result of the frequency response characteristics based on the circuit conditions; Fig. ~~12(a)~~ 12A is a circuit block diagram which illustrates an identical equivalent circuit to that shown in Fig. ~~11(a)~~ 11A; Fig. ~~12(b)~~ 12B is a graph which illustrates the simulation result based on circuit conditions shown in Fig. ~~12(a)~~ 12A; ~~Fig. 12(c)~~ 12C is a graph which illustrates the simulation result of frequency response characteristics in the equivalent circuit shown in Fig. ~~11(a)~~ 11A when an inductance L4 of a wire bond 23a (or 23b) is changed from 3 nanohenries to 1 nanohenry; Fig.~~13(a)~~ 13A illustrates an identical equivalent circuit to that shown in Fig. ~~11(a)~~ 11A; Fig. ~~13(b)~~ 13B is a graph which illustrates a simulation result based on circuit conditions shown in Fig. ~~13(a)~~ 13A; Fig. ~~13(c)~~ 13C is a graph which illustrates the simulation result of the frequency response characteristics when an inductance L1 of an inductance element is changed in the equivalent circuit shown in Fig .~~11(a)~~ 11A; Fig. 14 illustrates the outside configuration of the LD module which includes a can package and a receptacle; Fig. ~~15(a)~~ 15A is a horizontal sectional view (a view of a surface parallel to x shown in Fig. 14) of the LD module; Fig. ~~15(b)~~ 15B is a vertical sectional view (a view of a surface

parallel to y shown in Fig. 14) of the LD module; Fig. 16 is a perspective view which illustrates the can package in a state in which a cap is detached; Fig. ~~17(a)~~ 17A is a top view in a state in which an upper cap is detached; Fig. ~~17(b)~~ 17B is a cross-sectional view taken along a line II of Fig. ~~17(a)~~ 17A in a state in which the upper cap is attached; Fig. 18 is a circuit diagram which illustrates one example of a conventional single-phase feed type optical semiconductor device; Fig. 19 illustrates one example of an eye pattern of electric signal waveforms output from a circuit such as an LD driving circuit shown in Fig. 18; Fig. 20 illustrates one example of an eye pattern of optical signal waveforms (optical output waveforms) output from the LD module shown in Fig. 18; and Fig. 21 is a graph which illustrates the frequency response characteristics when a signal transmission path P between the LD driving circuit and the LD module shown in Fig. 18 is constituted by a distributed constant circuit such as a micro-strip line and when the LD module is viewed from this distributed constant circuit.

Please replace the paragraph beginning on page 22, line 10 and ending on page 22, line 14, with the following amended paragraph:

Fig. ~~2(a)~~ 2A is an explanatory view which typically illustrates rising and fall characteristics of the paired differential transistors 12 and 13 in the LD driving circuit 1. Fig.~~2(b)~~ 2B is an explanatory view which illustrates a principle that the rising and fall characteristics of the paired differential transistors 12 and 13 are average.

Please replace the paragraph beginning on page 22, line 15 and ending on page 22, line 18, with the following amended paragraph:

As shown in Fig. ~~2(a)~~ 2A, if a rise time of the differential transistor 12 or 13 (it is assumed that the transistors 12 and 13 are equivalent in characteristics) is tr and a fall time thereof is tf, tr and tf satisfies a relationship tr< tf. This is already explained above.

Please replace the paragraph beginning on page 23, line 13 and ending on page 23, line 21 with the following amended paragraph:

The circuits in the optical semiconductor device according to the present invention shown in Fig. 1 perform such as push-pull operation. Therefore, the distributed constant circuit 18 serves as differential lines, performs current push and pull for the LD 20 simultaneously. If the operation is viewed from the LD 20, the circuits operate for an average time ((tr + tf) / 2) between the rise time (tr) of the differential transistor 12 and the fall time (tf) of the differential transistor 13. As a result, as shown in Fig. ~~2(b)~~ 2B, the paired transistors 12 and 13 exhibit symmetric rise characteristics that the rise time and the fall time are averaged.

Please replace the paragraph beginning on page 25, line 10 and ending on page 26, line 3 with the following amended paragraph:

Fig. ~~4(a)~~ 4A is a graph which illustrates frequency response characteristics when the LD module 2 shown in Fig. 1 is viewed from the distributed constant circuit 18. As explained, the bias circuit 23a, in which the solenoid 21a and the resistor 22a are arranged in parallel, is connected to the cathode side of the LD 20 in the LD module 2 shown in Fig. 1, and the bias circuit 23b, in which the solenoid 21b and the resistor 22b are arranged in parallel, is connected to the anode side of the LD 20 in the LD module 2. Therefore, the respective bias circuits 28a

and 28b generate a resonance due to the capacitance components of the pad sections provided on the ceramic substrate or the like, similarly to the example of the conventional LD module 300. However, if the LD module 2 is viewed as an equivalent circuit from the distributed constant circuit 18 side, the two bias circuits appear as if they are connected in series. Therefore, an amplitude of the resonance can be reduced, and the sharp decline at the frequency around 10 gigahertz as shown in Fig. 21 is prevented. In the example shown in Fig. ~~4(a)~~ 4A the graph which illustrates the frequency response characteristics when the impedances of the resistors 22a and 22b are set equal is shown.

Please replace the paragraph beginning on page 26, line 4 and ending on page 26, line 9 with the following amended paragraph:

Fig. ~~4(b)~~ 4B is a graph which illustrates the frequency response characteristics when the bias circuits 28a and 28b are set to have different impedances. As shown in Fig. ~~4(b)~~ 4B, waviness is improved as compared with the graph of Fig. ~~4(a)~~ 4A. Specific examples of inductances and resistors will be explained later in the third and the fourth embodiments.

Please replace the paragraph beginning on page 32, line 20 and ending on page 33, line 2 with the following amended paragraph:

Fig. ~~6(a)~~ 6A is a top view of the filter 27, and Fig. ~~6(b)~~ 6B is an illustration of this filter 27 viewed from an arrow P direction. In Fig. ~~6(a)~~ 6A and Fig. ~~6(b)~~ 6B, the filter 27 includes a pair of micro-strip differential lines 39 on an upper surface of a ceramic substrate 41 and a

ground conductor 40 on a lower surface thereof. In addition, a comb-like strip conductor electrode 38 is formed alternately from the paired micro-strip conductor lines 39 in an inward direction orthogonal to the micro-strip conductor lines 39.

Please replace the paragraph beginning on page 33, line 3 and ending on page 33, line 15 with the following amended paragraph:

Fig. 7 is a graph which compares frequency response characteristics before and after insertion of the filter 27. In Fig. 7, C1 indicates the curve of Fig. ~~4(b)~~ 4B and indicates a waveform in which the waviness of the response characteristics is improved by setting the impedances of the bias circuits 28a and 28b shown in Fig. 5 asymmetric to each other. C2 is a waveform indicating the response characteristics if the peaking is applied to the LD driving circuit 1 shown in Fig. 5 by changing the circuit constant, not shown when a ringing at cycles of about 15 gigahertz occurs. C3 is a waveform which indicates the response characteristics when the ringing around 15 gigahertz is cut off by the filter 27. Fig. 7 shows that flat and good frequency response characteristics are obtained up to the frequency exceeding 12 gigahertz.

Please replace the paragraph beginning on page 33, line 16 and ending on page 33, line 24 with the following amended paragraph:

Japanese Patent Application Laid-Open Publication No. 7-38185 discloses, in ~~Fig. 6~~ Figs. 6A and 6B, a circuit in which serial circuits including a capacitance and a resistor are inserted in parallel to an LD element and which thereby prevents the ringing of rise

characteristics. An object of this circuit is, however, to remove an overshoot which occurs because no bias current is applied and a relaxation oscillation, which object differs from the object of the present invention. Further, the circuit of the publication differs from the present invention in that the circuit is a single-phase feed type and also differs in circuit configuration.

Please replace the paragraph beginning on page 33, line 25 and ending on page 34, line 6 with the following amended paragraph:

Japanese Patent Application Laid-Open Publication No. 7-46194 discloses, in Fig. 1 and ~~Fig. 2~~ Figs 2A and 2B, a circuit which changes a matching state by connecting, in parallel, serial circuits including an inductance and a resistor to an LD element between a matching resistor and an LD driving circuit, to thereby prevent a ringing. However, the invention differs from the present invention in object and circuit configuration and also differs in that the circuit is of a single-phase feed type.

Please replace the paragraph beginning on page 36, line 16 and ending on page 37, line 2 with the following amended paragraph:

Fig. ~~9(a)~~ 9A is a simplified equivalent circuit diagram which simulates a high frequency operation of the conventional optical semiconductor device shown in Fig. 18. In Fig. ~~9(a)~~ 9A, reference symbol 31 denotes the output impedance of the LD driving circuit, 309 denotes a matching resistor, and 310 denotes the internal resistance of the LD. Reference symbol 329 is the wire bond that connects pads, not shown in Fig. ~~9(a)~~ 9A, provided on the

conductor line electrically connected to the matching resistor 309 to the cathode of the LD 310. Reference symbol 32 denotes the bias circuit including the inductance element 311 such as the solenoid. Although the resistances should actually be reactances, the resistances are shown for simplifying explanation of fundamental passing characteristics in ~~Fig. 9 and Fig. 10~~ Figs. 9A, 9B, 10A, and 10B.

Please replace the paragraph beginning on page 37, line 3 and ending on page 37, line 11 with the following amended paragraph:

Fig. ~~9(b)~~ 9B is a graph which illustrates a simulation result of the frequency response characteristics of this equivalent circuit. Fig. ~~9(b)~~ 9B illustrates the simulation result when the output impedance Z1 of the LD driving circuit side is 50 ohms, the internal resistance r1 of the LD 310 is 8 ohms, the resistance R3 of the matching resistor 309 is 40 ohms, the inductance L of the wire bond 329 is 0.5 nanohenries, and the impedance of the bias circuit 32 is 50 ohms. Fig. ~~9(b)~~ 9B demonstrates that a 3-decibel band (between ml and m2 where the frequency is lower by 3 decibels than that of m1) is at about 10.6 gigahertz.

Please replace the paragraph beginning on page 37, line 12 and ending on page 37, line 18 with the following amended paragraph:

Fig. ~~10(a)~~ 10A is a simplified equivalent circuit diagram which simulates the high frequency operation of the optical semiconductor device (differential lines) according to the present invention shown in Fig. 1. In Fig. ~~10(a)~~ 10A, reference symbol 31 denotes the output

impedance of the LD driving circuit, 19a and 19b denote the matching resistors, 20 denotes the LD, 29 denotes the wire bond, and 32 and 33 denote the respective bias circuits.

Please replace the paragraph beginning on page 37, line 19 and ending on page 38, line 3 with the following amended paragraph:

Fig. ~~10(b)~~ 10B is a graph which illustrates a simulation result of the frequency response characteristics of this equivalent circuit. Fig. ~~10(b)~~ 10B illustrates the simulation result when the output impedance Z1 of the LD driving circuit side is 100 ohms, the internal resistance rl of the LD 20 is 8 ohms, the resistances R3 of the matching resistors 19a and 19b are 40 ohms, the inductance L of the wire bond 29 is 0.5 nanohenry, and the impedances of the bias circuits 32 and 33 are 50 ohms. Fig. ~~10(b)~~ 10B demonstrates that a 3-decibel band (between m3 and m4 where the frequency is lower by 3 decibels than that of m3) is at about 18.6 gigahertz.

Please replace the paragraph beginning on page 38, line 19 and ending on page 39, line 1 with the following amended paragraph:

Fig. ~~11(a)~~ 11A is a circuit diagram which illustrates the configuration of the bias circuits in the equivalent circuit shown in Fig. ~~10(a)~~ 10A in detail. Since the configuration and operation of this equivalent circuit are the same as those explained in the first embodiment, they will not be explained herein. In this fourth embodiment, the characteristics of the equivalent circuit in the first embodiment will be explained while referring to specific examples of inductances, capacitances, and resistances.

Please replace the paragraph beginning on page 39, line 4 and ending on page 39, line 15 with the following amended paragraph:

Pieces of data on the respective elements of the equivalent circuit of the optical semiconductor device in the first specific example are as follows if using symbols shown in Fig. ~~11(a)~~ 11A. Resistances R1 and R2 of the resistors 22a and 22b are 1,000 ohms, resistances R3 and R4 of the matching resistors 19a and 19b are 40 ohms, inductances Ll and L2 of the solenoids 21a and 21b are 0.5 nanohenry, inductances L4 and L5 of the wire bonds 23a and 23b are 3 nanohenries, the resistance Z1 of the LD driving circuit side is 100 ohms, the resistance r1 of the LD 20 is 8 ohms, and parasitic capacitances Cl, C2, C3, and C4 of the bias circuits are 0.1 picofarad. Fig. ~~11(b)~~ 11B is a graph which illustrates a simulation result of the frequency characteristics based on these circuit conditions.

Please replace the paragraph beginning on page 39, line 16 and ending on page 40, line 2 with the following amended paragraph:

Fig. ~~11(c)~~ 11C is a circuit block diagram which illustrates the configuration of the bias circuits in the equivalent circuit shown in Fig. ~~9(a)~~ 9A in detail. Since the configuration and operation of this equivalent circuit are the same as those explained in the conventional art, they will not be explained herein. Pieces of data on the respective elements of the equivalent circuit are as follows if using symbols shown in Fig. ~~11(c)~~ 11C. R2 is 1,000 ohms, R3 is 40 ohms, the inductance L2 of the inductance element 311 is 100 nanohenries, L3 = 0.5 nanohenry, L5 = 3 nanohenries, and the parasitic capacitances C2 and C4 of the bias circuits are 0.1 picofarad. Fig.

~~11(d)~~ 11D is a graph which illustrates a simulation result of the frequency characteristics based on these circuit conditions.

Please replace the paragraph beginning on page 40, line 3 and ending on page 40, line 14 with the following amended paragraph:

As shown in the simulation results of Fig. ~~11(b)~~ 11B and Fig. ~~11(d)~~ 11D, if the optical semiconductor device employs the differential feed type bias circuits, the amplitude of the resonance ripple caused by the bias circuits can be reduced, as compared with the device that employs the single-phase feed type bias circuits. The result of Fig. ~~11(b)~~ 11B corresponds to that of Fig. ~~4(a)~~ 4A which illustrates the experimental result of the differential feed type optical semiconductor device in the first embodiment, and that of Fig. ~~11(d)~~ 11D corresponds to that of Fig. 21 which illustrates the experimental result of the single-phase feed type optical semiconductor device. It is noted, however, that the experimental results of Fig. ~~4(a)~~ 4A and Fig. 21 include the frequency characteristics of the LD driving circuits 1 and 200 and a high frequency region is cut off.

Please replace the paragraph beginning on page 41, line 3 and ending on page 41, line 9 with the following amended paragraph:

Fig. ~~12(a)~~ 12A is a circuit block diagram which illustrates the identical equivalent circuit to that shown in Fig. ~~11(a)~~ 11A. Fig. ~~12(b)~~ 12B is a graph which illustrates a simulation result based on circuit conditions shown in Fig. ~~12(a)~~ 12A, and corresponds to the graph shown

in Fig. ~~11(b)~~ 11B. Fig. ~~12(c)~~ 12C is a graph which illustrates a simulation result of the frequency response characteristics when the inductance L4 of the wire bond 23a (or 23c) is changed from 3 nanohenries to 1 nanohenry.

Please replace the paragraph beginning on page 41, line 10 and ending on page 41, line 16 with the following amended paragraph:

As shown in the simulation results of Fig. ~~12(b)~~ 12B and Fig. ~~12(c)~~ 12C, by making the inductance components of the wire bond connecting the bias circuit to the LD element and the like asymmetric vertically, a frequency at which the resonance ripple occurs can be set high. Although the amplitude of the ripple increases, a region in which the ripple occurs can be forced out of the band. Therefore, this is advantageous when a desired band is to be secured.

Please replace the paragraph beginning on page 41, line 23 and ending on page 42, line 8 with the following amended paragraph:

Fig. ~~13(a)~~ 13A is a circuit block diagram which illustrates the identical equivalent circuit to that shown in Fig. ~~11(a)~~ 11A. Fig. ~~13(b)~~ 13B is a graph which illustrates a simulation result based on circuit conditions shown in Fig. ~~13(a)~~ 13A, and corresponds to the graph shown in Fig. ~~11(b)~~ 11B. Fig. ~~13(c)~~ 13C is a graph which illustrates a simulation result of the frequency response characteristics when the inductance L1 of the solenoid 21a is changed in the equivalent circuit of Fig. ~~11(a)~~ 11A. As regards the solenoid 21a and the resistance 22a, Fig. ~~13(b)~~ 13B is the graph before the inductance Ll is changed while setting Ll = 100 nanohenries

and R1 = 1,000 ohms, and Fig. ~~13(c)~~ 13C is the graph after the inductance Ll is changed while setting Ll = 10 nanohenries and R1 = 400 ohms.

Please replace the paragraph beginning on page 42, line 9 and ending on page 42, line 17 with the following amended paragraph:

As shown in the simulation results of Fig. ~~13(b)~~ 13B and Fig. ~~13(c)~~ 13C, by making the impedances of the solenoid 21a (or 21b) and the resistor 22a (or 22b) connected in parallel to each other in the bias circuit asymmetric vertically, the amplitude of the resonance ripple can be further reduced. This is the same in content as that shown in the experimental result of Fig. ~~4(b)~~ 4B which illustrates the first embodiment. In the experimental result of Fig. ~~4(b)~~ 4B which illustrates the first embodiment, the frequency characteristics of the LD driving circuit 1 are included and the high frequency region is cut off.

Please replace the paragraph beginning on page 43, line 17 and ending on page 43, line 24 with the following amended paragraph:

As shown in Fig. 14 and ~~Fig. 15~~ Figs. 15A and 15B, the can package 101 includes a disk-like stem 110 on which bias feed pins (144a, 144b), high frequency signal pins (141a, 141b), and the like are mounted, a trapezoidal pedestal 111 (a pedestal block) on which a plurality of ceramic substrates are mounted, the condenser lens 25 which condenses a laser light emitted from the LD 20, a cylindrical cap 113 which airtight seals the pedestal 111 and the like from the outside, and the like.

Please replace the paragraph beginning on page 43, line 25 and ending on page 44, line 10 with the following amended paragraph:

As shown in ~~Fig. 15~~ Figs. 15A and 15B, the cap 113 has a double cylinder form which includes a first cap member 113a fixed to the stem 110 by projection welding or the like and a second cap member 113b fitted into a tip end side of the first cap member 113a from outward and fixed to the first cap member 113a by YAG welding or the like. Specifically, the first cap member 113a includes stepped outer cylinders, and the outer cylinder having a smaller diameter is provided on the tip end of the outer cylinder having a larger diameter. An inner cylinder of the one end-side second cap member 113b is fitted into the outer periphery of the outer cylinder having the smaller diameter, and the first cap member 113a is fixed to the second cap member 113b by through YAG welding.

Please replace the paragraph beginning on page 58, line 18 and ending on page 58, line 23 with the following amended paragraph:

The optical semiconductor element module in the sixth embodiment of the present invention will be explained with reference to ~~Fig. 17~~ Figs. 17A and 17B. Fig. ~~17(a)~~ 17A is a top view of the optical semiconductor element module in a state in which an upper cap 401 is detached, and Fig. ~~17(b)~~ 17B is a cross-sectional view taken along II of Fig. ~~17(a)~~ 17A (note, however, that Fig. ~~17(b)~~ 17B is in a state in which the upper cap 401 is attached).

Please replace the paragraph beginning on page 59, line 4 and ending on page 59, line 12 with the following amended paragraph:

As shown in ~~Fig. 17~~ Figs. 17A and 17B, in this optical semiconductor package 402, the positive-phase and antiphase differential signals are input to the input buffer 11 of the LD driving circuit 1 as already explained. To input the differential signals to the LD driving circuit 1 in the optical semiconductor package 402, the dielectric 177 (feed-through) is fitted into a sidewall of the optical semiconductor package 40, and the differential signals are transmitted through differential lines 178a and 178b provided on the dielectric 177 while keeping an interior and an exterior of the package airtight.

Please replace the Abstract with the following amended Abstract: